IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:
James E. King
Martin P. Mayhead

§ Group Art Unit: 2863
§
§ Examiner: Cherry, Stephen J.
§
§ Atty. Dkt. No.: 5681-71200
§ P8871

Serial No. 10/653,034

Filed: August 29, 2003

For: System Health Monitoring

CERTIFICATE OF MAILING
37 C.F.R. § 1.8

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Mario J. Lewin
Name of Registered Representative

11-14-05
Date

Signature

APPEAL BRIEF

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Alexandria, VA 22313-1450

Sir/Madam:

Further to the Notice of Appeal filed September 13, 2005, Appellant presents this Appeal Brief. Appellant respectfully requests that this appeal be considered by the Board of Patent Appeals and Interferences.

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I. REAL PARTY IN INTEREST

The subject application is owned by Sun Microsystems, Inc., a corporation organized and existing under and by virtue of the laws of the State of Delaware, and having its principal place of business at 4150 Network Circle, Santa Clara, CA 95054, as evidenced by the assignment recorded at Reel 015023, Frame 0303.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-35 are pending in the present application and Claims 1-9, 12-22, 25-26, and 29-35 are the subject of this appeal. Claims 1-9, 12, 14-22, 25, 29-32, and 34-35 stand finally rejected under 35 U.S.C. § 102(e). Claims 13, 26, and 33 stand finally rejected under 35 U.S.C. § 103(a). Claims 10-11, 23-24, and 27-28 stand objected. A copy of Claims 1-9, 12, 14-22, 25, 29-32, and 34-35, as on appeal (incorporating all amendments), is included in the Appendix hereto.

IV. STATUS OF AMENDMENTS

No amendment to the claims has been filed subsequent to the final rejection. The Appendix hereto reflects the current state of the claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In one embodiment, a method may be implemented for monitoring the health of a system module in a system during state transitioning. The system includes a monitor module operationally connected to the system module. The method may include the system module outputting a status signal at predetermined system status points during

state transitioning. The method may further include the monitor module starting a timer on detecting a first status signal and resetting the timer on detecting a subsequent status signal. The timer may indicate a failed transitioning of the system module in the event that the timer is not reset within a determined period. Therefore, a failed transitioning of a system module, e.g., a failed restart of a system module, may be detected, thereby enhancing the reliability of the overall system. *See* page 63, line 21 – page 78, line 12, and Figure 19-23.

In one embodiment, the state transitioning may take place, for example, when the system module is turned on and when the system module is shut down. A status signal may be output by the system module for at least one of the following system status points, namely: at power on self test start; at power on self test end; at power on or reset; at an end of initial hardware power up, at the start of booting, at completion of booting, on a shutdown or panic power-off, and on a system reset. *See* page 66, line 10 – page 68, line 22, and Figure 20.

In one embodiment, an initial period for the timer may be determined to exceed an expected maximum time to a subsequent status signal assuming a healthy system module. The monitor module may record a time for a given pair of status signals on a given initiation of the system and may adapt the determined period for a subsequent system initiation. The monitor module may also use information about the configuration of the system module to compute a determined period to be applied for the timer. *See* page 71, line 24 – page 77, line 13, and Figure 22.

VI. GROUNDS OF REJECTION

1. Claims 1-9, 12, 14-22, 25, 29-32, and 34-35 stand finally rejected under 35 U.S.C. § 102(e) as being anticipated by Gurumoorthy et al. (U.S. Patent No. 6,829,725).
2. Claims 13, 26, and 33 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Gurumoorthy et al. in view of Crippen et al. (U.S. Patent No. 6,688,965).

VII. ARGUMENT

A. Claims 1, 3, 6-9, 13-14, 16, 19-22, 26, 29, and 31-35

The Examiner rejected claims 1, 3, 6-9, 14, 16, 19-22, 29, 31-32, and 34-35 under 35 U.S.C. § 102(e) as being anticipated by Gurumoorthy et al. (U.S. Patent No. 6,829,725). The Examiner rejected claims 13, 26, and 33 under 35 U.S.C. § 103(a) as being unpatentable over Gurumoorthy et al. in view of Crippen et al. (U.S. Patent No. 6,688,965). Appellant respectfully traverses these rejections in light of the following remarks.

Gurumoorthy discloses a system and method of launching an operating system (OS). A firmware interface may be initially launched on a computer system. The firmware interface may comprise logic to attempt launching an operating system using an OS loader. Upon detection that the attempt is unsuccessful, the computer system may be automatically reset.

Appellant respectfully submits that Gurumoorthy fails to teach or suggest "A method of monitoring the health of a system module in a system during state transitioning...the method comprising: the system module outputting a status signal for predetermined system status points during state transitioning of the system module" as recited by claim 1 (emphasis added). The Examiner contends that these features are taught in column 6, line 21 and line 42 of Gurumoorthy. Appellant respectfully disagrees. Gurumoorthy teaches:

> At block 210, the OS loader may set a watchdog timer to a prespecified time interval, attempt to launch an operating system, and wait at diamond 212 for either a detection of a successful launch of the operating system at block 214 or an unsuccessful attempt at block 218. (Column 6, Lines 20-24)
>
> Block 218 detects an unsuccessful attempt to launch when the watchdog timer expires before the operating system has been launched (i.e., the

processing system is considered to be "frozen"). Upon detection of such an unsuccessful attempt, block 220 initiates a system reset at block 202. Otherwise, if the operating successfully launches before the watchdog timer expires, block 214 may disable the watchdog timer and terminate the OS loader before the operating system takes control of the processing platform at block 216. In the illustrated embodiment, block 214 may detect a successful launch of an operating system by, for example, detecting the completion of one more tasks initiated by the OS loader and the absence of one or more error conditions. (Column 6, Lines 37-49)

While Gurumoorthy teaches "the OS loader...attempting to launch an operating system" and "operating successfully launches", Gurumoorthy fails to teach or suggest "**system module outputting a status signal for predetermined system status points during state transitioning of the system module**" as recited by claim 1.

Additionally, Appellant respectfully submits that Gurumoorthy fails to teach or suggest "the monitor module being operable to start a timer on detecting a first status signal and resetting the timer on detecting a subsequent status signal" as recited by claim 1 (emphasis added). The Examiner contends that these features are taught in column 6, line 20 of Gurumoorthy (see above).

While Gurumoorthy teaches "the OS loader may set a watchdog timer to a prespecified time interval, attempt to launch an operating system, and wait at diamond 212 for either a detection of a successful launch of the operating system at block 214 or an unsuccessful attempt at block 218", Gurumoorthy fails to teach "**the monitor module being operable to start a timer on detecting a first status signal**" and "**the monitor module being operable to...resetting the timer on detecting a subsequent status signal**" as recited in claim 1. In fact, Gurumoorthy teaches away from this feature in that "if the operating successfully launches before the watchdog timer expires, block 214 may **disable** the watchdog timer". (Gurumoorthy , Column 6, Line 42-44) (Emphasis added)

The Examiner further contends that the system "at block 210 sets the watchdog

timer for each iteration of the depicted loop, wherein block 220 is looped back to block 202. Thus, a second iteration of the depicted flowchart would involve a resetting of the watchdog timer", and "The condition of operating system successfully loading is monitored in each successive iteration instruction 212 in the disclosed programming loop, thereby demonstrating claimed first status signal and subsequent status signal." Appellant respectfully disagrees.

Appellant reminds the Examiner that anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Gurumoorthy does not teach or suggest the outputting and detecting of status signals for predetermined system status points during state transitioning of a system module. Specifically, Gurumoorthy does not teach or suggest that the OS loader or operating system of Gurumoorthy outputs status signals for predetermined system status points during state transitioning. In particular, there is no teaching or suggestion in Gurumoorthy for a system module outputting a first status signal (for a predetermined system status point) and a monitor module starting a timer on detecting the first status signal. Additionally, there is no teaching or suggestion in Gurumoorthy for the system module outputting a subsequent status signal (for another predetermined system status point) and the monitor module resetting the timer on detecting the subsequent status signal.

Furthermore, Gurumoorthy does not teach or suggest a monitor module which is operable to start and reset the timer. Gurumoorthy discloses an OS loader in the firmware but does not teach or suggest a system module, operationally connected to a monitor module, which undergoes state transitioning.

In accordance, claim 1 is believed to patentably distinguish over the cited reference. Claims 3 and 6-9 depend on claim 1 and are therefore believed to patentably distinguish over the cited reference for at least the reasons given above.

Claims 14, 29, and 34-35 recite features similar to those highlighted above with regard to independent claim 1 and are thus also believed to patentably distinguish over the cited reference for at least the same reasons given above. Claims 16 and 19-22 depend on claim 14 and claims 31-32 depend on claim 29, and are therefore believed to patentably distinguish over the cited reference for at least the same reasons.

Since the rejection is not supported by the teaching of the cited reference, Appellant respectfully requests reversal of the Examiner's rejection of Claims 1, 3, 6-9, 14, 16, 19-22, 29, 31-32, and 34-35.

B. Claims 2, 15, and 30

The Examiner rejected claims 2, 15, and 30 under 35 U.S.C. § 102(e) as being anticipated by Gurumoorthy. Appellant respectfully traverses these rejections in light of the following remarks.

The rejection of claims 2, 15, and 30 is unsupported by the cited reference for at least the reasons given above in Argument A. Furthermore, contrary to the Examiner's assertion, Gurumoorthy fails to teach or suggest "wherein the state transitioning comprises at least one of starting the **system module** and shutting down the **system module**" as recited in claims 2, 15, and 30.

The Examiner contends that these features are taught in column 6, line 20 of Gurumoorthy (cited above). Appellant respectfully disagrees. Gurumoorthy discloses an

OS loader in the firmware but does not teach or suggest a system module, operationally connected to a monitor module, which undergoes state transitioning.

In accordance, claims 2, 15, and 30 are believed to patentably distinguish over the cited reference. Since the rejection is not supported by the teaching of the cited reference, Appellant respectfully requests reversal of the Examiner's rejection of claims 2, 15, and 30.

C. Claims 4 and 17

The Examiner rejected claims 4 and 17 under 35 U.S.C. § 102(e) as being anticipated by Gurumoorthy et al. Appellant respectfully traverses these rejections in light of the following remarks.

The rejection of claims 4 and 17 are unsupported by the cited reference for at least the reasons given above in Argument A. Additionally, Gurumoorthy fails to teach or suggest "wherein the timer is reset on detecting each of **a set** of successive status signals, whereby the timer is operable to indicate a failed transitioning of the system module in the event that the timer is not reset within a respective determined period for each of **a plurality of pairs** of successive status signals" as recited in claims 4 and 17.

In accordance, claims 4 and 17 are believed to patentably distinguish over the cited reference. Since the rejection is not supported by the teaching of the cited reference, Appellant respectfully requests reversal of the Examiner's rejection of claims 4 and 17.

D. Claims 5 and 18

The Examiner rejected claims 5 and 18 under 35 U.S.C. § 102(e) as being anticipated by Gurumoorthy et al. Appellant respectfully traverses these rejections in light of the following remarks.

The rejection of claims 5 and 18 are unsupported by the cited reference for at least the reasons given above in Argument A. Furthermore, Gurumoorthy fails to teach or suggest "wherein an initial period for the timer is determined to exceed an expected maximum time to a subsequent status signal assuming a healthy system module" as recited in claims 5 and 18.

In accordance, claims 5 and 18 are believed to patentably distinguish over the cited reference. Since the rejection is not supported by the teaching of the cited reference, Appellant respectfully requests reversal of the Examiner's rejection of claims 5 and 18.

E. Claims 12 and 25

The Examiner rejected claims 12 and 25 under 35 U.S.C. § 102(e) as being anticipated by Gurumoorthy et al. Appellant respectfully traverses these rejections in light of the following remarks.

The rejection of claims 12 and 25 are unsupported by the cited reference for at least the reasons given above in Argument A. Additionally, Gurumoorthy fails to teach or suggest "wherein the monitor module is a service processor" as recited in claims 12 and 25.

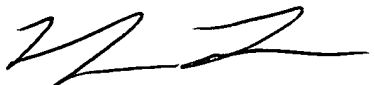
In accordance, claims 12 and 25 are believed to patentably distinguish over the cited reference. Since the rejection is not supported by the teaching of the cited reference, Appellant respectfully requests reversal of the Examiner's rejection of claims 12 and 25.

VIII. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejections of claims 1-9, 12-22, 25-26, and 29-35 were erroneous, and reversal of Examiner's decision is respectfully requested.

The Commissioner is authorized to charge the appeal brief fee of $330.00 and any other fees that may be due to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-71200/BNK. This Appeal Brief is submitted in triplicate along with a return receipt postcard.

Respectfully submitted,



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IX. CLAIMS APPENDIX

The claims on appeal are as follows.

1. A method of monitoring the health of a system module in a system during state transitioning, wherein the system further includes a monitor module operationally connected to the system module, the method comprising:
   - the system module outputting a status signal for predetermined system status points during state transitioning of the system module; and
   - the monitor module being operable to start a timer on detecting a first status signal and resetting the timer on detecting a subsequent status signal, whereby the timer is operable to indicate a failed transitioning of the system module in the event that the timer is not reset within a determined period.

2. The method of claim 1, wherein the state transitioning comprises at least one of starting the system module and shutting down the system module.

3. The method of claim 1, wherein a signal is output by the system module for at least one of the following system status points, namely: at power on self test start; at power on self test end; at power on or reset; at an end of initial hardware power up, on starting booting, on ending booting, on a shutdown or panic power-off and on a system reset.

4. The method of claim 1, wherein the timer is reset on detecting each of a set of successive status signals, whereby the timer is operable to indicate a failed transitioning of the system module in the event that the timer is not reset within a respective determined period for each of a plurality of pairs of successive status signals

5. The method of claim 1, wherein an initial period for the timer is determined to exceed an expected maximum time to a subsequent status signal assuming a healthy system module.

6. The method of claim 5, wherein the monitor module is operable to set the configuration of the system module, and wherein the monitor module is operable to use information about the configuration to compute a determined period to be applied for the timer.

7. The method of claim 5, wherein the system module is operable to inform the monitor module of a determined period to be applied for the timer.

8. The method of claim 5, wherein the system module is operable to provide the monitor module with details of the configuration of the system module, and wherein the monitor module is operable to use the configuration information to compute a determined period to be applied for the timer.

9. The method of claim 5, wherein the monitor module is operable to interrogate the system module to determine details of the configuration of the system module, and wherein the monitor module is operable to use the configuration information to compute a determined period to be applied for the timer.

12. The method of claim 1, wherein the monitor module is a service processor.

13. The method of claim 12, wherein the service processor is a shelf service processor for a shelf of a rack mountable blade system and at least one said system module is a processor blade receivable in the shelf.

14. A computer system configured to receive a system module and comprising a monitor module operationally to be connected to the system module, wherein:

- the monitor module is operable to start a timer on detecting a first status signal output by a received system module at one of predetermined system status points during state transitioning of the system module; and
- the monitor module is operable to reset the timer on detecting a subsequent status signal output by a received system module at another predetermined system status point during state transitioning of the system module, whereby the timer is operable to indicate a failed transitioning of the system module in the event that the timer is not reset within a determined period.

15. The computer system of claim 14, wherein the state transitioning comprises at least one of starting the system module and shutting down the system module.

16. The computer system of claim 14, wherein the monitor module is responsive to signals output by a received system module for at least one of the following system status points, namely: at power on self test start; at power on self test end; at power on or reset; at an end of initial hardware power up, on starting booting, on ending booting, on a shutdown or panic power-off and on a system reset.

17. The computer system of claim 14, wherein the timer is operable to be reset on detecting each of a set of subsequent status signals, whereby the timer is operable to indicate a failed transitioning of the system module in the event that the timer is not reset within a respective determined period for each of a plurality of pairs of successive status signals

18. The computer system of claim 14, wherein an initial period for the timer is determined to exceed an expected maximum time to a subsequent status signal assuming a healthy system module.

19. The computer system of claim 18, wherein the monitor module is operable to set the configuration of the system module, and wherein the monitor module is

operable to use information about the configuration to compute a determined period to be applied for the timer.

20. The computer system of claim 18, wherein the monitor module is responsive to a system module providing a determined period to be applied for the timer.

21. The computer system of claim 18, wherein the monitor module is responsive to a system module providing details of the configuration of the system module, and wherein the monitor module is operable to use the configuration information to compute a determined period to be applied for the timer.

22. The computer system of claim 18, wherein the monitor module is operable to interrogate the system module to determine details of the configuration of the system module, and wherein the monitor module is operable to use the configuration information to compute a determined period to be applied for the timer.

25. The computer system of claim 14, wherein the monitor module is a service processor.

26. The computer system of claim 25, wherein the service processor is a shelf service processor for a shelf of a rack mountable computer system.

29. A system module for a computer system configured to receive said system module and comprising a monitor module to be operationally connected to the system module, the system module being operable to output status signals at predetermined system status points during state transitioning of the system module, whereby the monitor module is operable to set a time on receipt of a first such status signal and to reset the timer on detecting a subsequent status signal,

and whereby the timer is operable to indicate a failed transitioning of the system module in the event that the timer is not reset within a determined period.

30. The system module of claim 29, wherein the state transitioning comprises at least one of starting the system module and shutting down the system module.

31. The system module of claim 29, wherein the system module is operable to output a status signal for at least one of the following system status points, namely: at power on self test start; at power on self test end; at power on or reset; at an end of initial hardware power up, on starting booting, on ending booting, on a shutdown or panic power-off and on a system reset.

32. The system module of claim 29, wherein the system module is operable to provide the monitor module with an indication of the determined period to be applied for the timer.

33. The system module of 29, wherein the system module is a server blade for a rack mountable blade server system.

34. A carrier medium carrying instructions for monitoring the health of a system module in a system during power transitioning, wherein a monitor module is operationally connected to the system module and the system module is operable to output a status signal at predetermined system status points during at least one of starting the system module and shutting down the system module, the instructions being operable to control the monitor module:

- to start a timer on detecting a first status signal; and
- to reset the timer on detecting a subsequent status signal, whereby the timer is operable to indicate a failed transitioning of the system module in the event that the timer is not reset within a determined period.

35. A computer system comprising a system module and a monitor module operationally connected to the system module, wherein:

- the system module comprises means for outputting a status signal for predetermined system status points during state transitioning of the system module; and
- the monitor module comprises means for start a timer on detecting a first status signal and for resetting the timer on detecting a subsequent status signal, whereby the timer is operable to indicate a failed transitioning of the system module in the event that the timer is not reset within a determined period.

X. EVIDENCE APPENDIX

None

X. RELATED PROCEEDINGS APPENDIX

None

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
King, et al.

Serial No.: 10/653,034

Filed: August 29, 2003

For: SYSTEM HEALTH MONITORING

§ Group Art Unit: 2863
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§ Examiner: Stephen J. Cherry
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§ Atty. Dkt. No. 5681-71200
§

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below:

Mario J. Lewin
Registered Representative

November 14, 2005 _____
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FEE AUTHORIZATION

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Attorney Docket No.:	5681-71200

The Commissioner is also authorized to charge any extension fee or other fees which may be necessary to the same account number.

Respectfully submitted,

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